A SINGLE-BIAS DIODE-REGULATED 60GHZ MONOLITHIC LNA

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Abstract

This paper presents a small-size 60GHz-band GaAs MMIC LNA with a single bias supply. A diode-regulated self-bias circuit was proposed and demonstrated for suppressing the FET drain current variations due to threshold voltage nonuniformities. The developed three-stage MMIC LNA exhibited an average noise figure of 3.3dB with 18dB gain from 58 to 62GHz. The chip size of the LNA is 1.85mm $\times$ 1.07mm $\times$ 0.04mm.

I Introduction

To date, several applications such as wireless LANs, cordless cameras and contactless ID card systems[1] have been proposed and tested for 60GHz-frequency-band. An MMIC LNA is a key element for RX modules in the above mentioned systems. A self-biased LNA is useful because it requires only one positive voltage source and simplifies bias networks for MMIC design. Recently, self-biased MMIC LNAs have been reported at C- and X-bands[2]-[4], however to our knowledge, there have been no reports for single-bias monolithic LNAs operating at higher frequency-bands. For a high transconductance millimeter-wave FET, the drain current is sensitive to threshold voltage variations due to nonuniformities in the wafers and the gate recess process. Therefore, it is important for a self-biased LNA to regulate the drain current.

This paper describes a small-size 60GHz-band GaAs-based MMIC LNA operating with a single bias supply introducing a diode-regulated self-bias circuit. Using this bias circuit, the sensitivity of the drain current to the FET threshold voltage variations was reduced to 58% compared to that for a conventional self-bias circuit.

II Circuit Design

An equivalent circuit for the three-stage LNA is shown in Fig.1. In the circuit, 0.15μm$\times$60μm AlGaAs/InGaAs heterojunction FETs(HJFETs) were employed. The typical threshold voltage of the FET was -0.9V. The amplifier consists of three noise-matched, identical stages. Each stage has been designed to be unconditionally stable by incorporating series feedback lines for the source terminal and RC bias networks for the drain terminal of the FET. At all frequencies, a stability factor K$>$2 for the overall three-stage amplifier was realized.

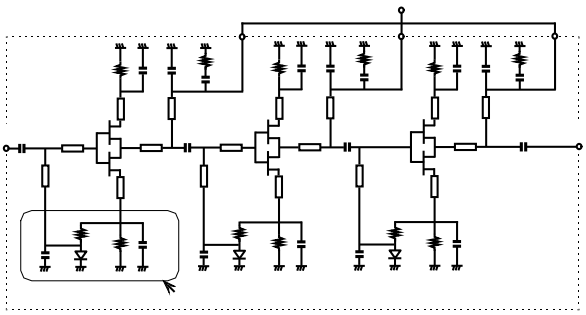

Fig. 1. Circuit topology for the designed self-biased three-stage monolithic amplifier.

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For the gate bias network, a diode-regulated self-bias circuit as shown in Fig.2(a) has been introduced to reduce the drain current sensitivity to the FET threshold voltage(Vth) variations. In the circuit, a Shottky diode forward turn-on voltage, Vf, is applied to the gate voltage(Vg). A current limiting resistor and the diode are connected in series between the source terminal of the FET and the ground.

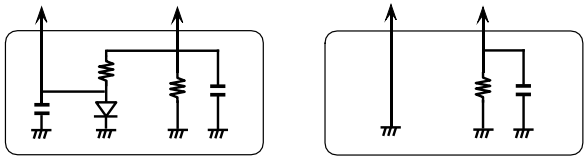

Fig. 2. Diagrams for (a) a diode-regulated self-bias circuit used in Fig.1., and (b) a conventional self-bias circuit.

The drain current distributions(σ) for the proposed and for a simple bias circuit[2] shown in Fig.2(b) were evaluated on a 3-inch wafer. As shown in Fig.3, the drain current distribution for the proposed bias circuit(Vg=Vf) was 58% compared to that for the conventional circuit(Vg=0). This can be explained by a resistor value(R) between the source terminal and the ground. Since drain current(Id) near pinch-off region is approximately described as $Id = \beta(Vg - Vth - R \cdot Id)^2$, R for a set current($Id^{SET}$) can be described as:

$$R = \frac{1}{Id^{SET}} \left(Vg - Vth - \sqrt{\frac{Id^{SET}}{\beta}} \right), \qquad (1)$$

where β is a fitting factor for FET Id v.s. Vg characteristics. Thus, R is larger(R=460Ω) for the proposed circuit than that for the conventional circuit(R=190Ω). As a result, a transconductance including this resistor, which is equal to $-(\partial Id)/(\partial Vth)$ [2], is smaller at the same designed drain current.

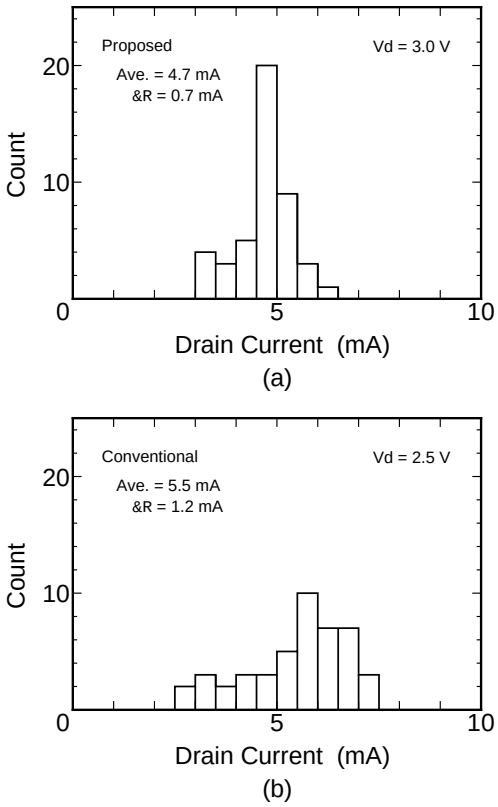

Fig. 3. Drain current distributions(single-stage) over a wafer for (a) the diode-regulated self-bias circuit and (b) the conventional self-bias circuit.

Besides the drain current sensitivity reduction, this bias circuit facilitates realization of a simple small-size MMIC because it does not need active elements for current regulation or long bias lines from drain(dc pad) to gate bias circuits across an RF signal line in a compact layout design. With a drain current of 5mA/stage at 3V, the total dc power consumption was estimated to be 45mW.

III MMIC Process and Device Characteristics

The epitaxial layer structure for an HJFET consists of an AlGaAs buffer layer, a 13nm undoped $In_{0.2}Ga_{0.8}As$ channel layer, a 33nm $Al_{0.2}Ga_{0.8}As$ layer with $5\times10^{12}cm^{-2}$ Si-planar

doping and an 80nm n^+-GaAs cap layer.

In FET fabrication, mesa-isolation, wet recess etching, electron beam evaporation and lift-off techniques were employed. Details were reported elsewhere[5][6]. The junction between HJFET gate and source(drain) terminals was used as a Shottky diode. A Metal-Insulator-Metal(MIM) structure with an SiN film as a dielectric layer was applied for fabricating both dc blocking and bypass capacitors. N^+ bulk resisters were used in the bias networks.

The HJFET has a T-shaped gate with 0.15μm length. The device exhibited a typical transconductance of 510mS/mm and an f_{max} of 200GHz at Vds=2V with a reverse gate-drain breakdown voltage of 10V. The measured minimum noise figure for the device was 0.4dB at 12GHz with an associated gain of 13dB.

IV MMIC Performance

The chip photograph for the monolithic three-stage LNA is shown in Fig.4. The chip size is 1.85mm $\times$ 1.07mm $\times$ 0.04mm.

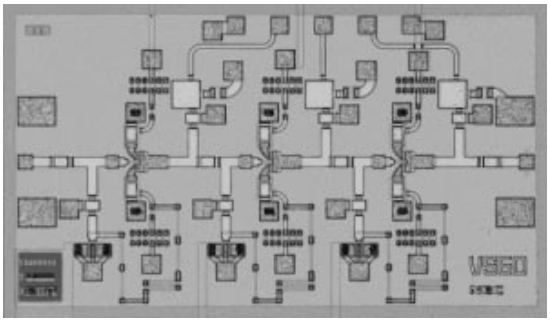

Fig. 4. Chip photograph for the fabricated three-stage MMIC LNA (1.85mm $\times$ 1.07mm).

Ten MMIC chips were tested by on-wafer RF probes. At a supply voltage(Vd) of 3V, drain currents were at a range from 3.5 to 5.1mA/stage. The measured noise figure and gain as a function of frequency are represented in Fig.5. Noise figure variation at 60GHz was from 3.2 to 3.7dB and gain variation was from 17.2 to 18.3dB. For the best chip, the average noise figure from 58 to 62GHz was 3.3dB with 18dB gain.

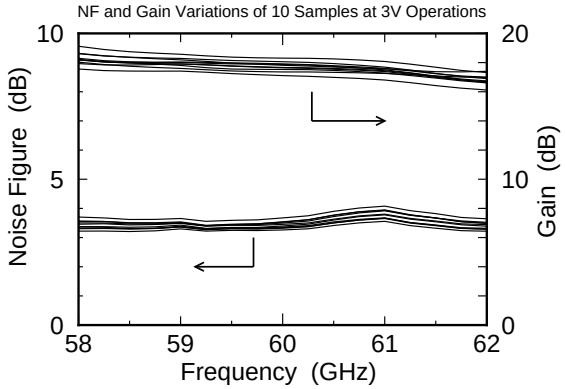

Fig. 5. Measured noise figure and gain of ten MMIC LNAs at 3V.

The measured noise figure and gain of the LNA as a function of supply voltage are shown in Fig.6. When the drain voltage was increased from 3 to 5V, the drain current gradually increased only by 10%. At this time, the noise figure was almost unchanged with a gain of 16dB at 60GHz.

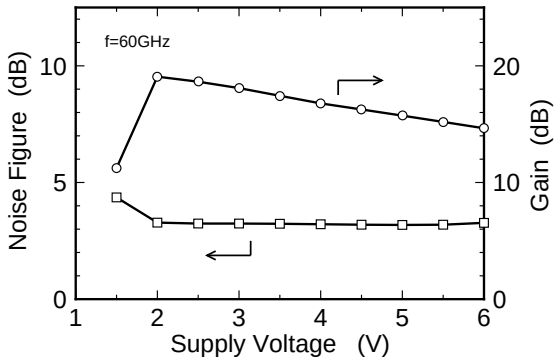

Fig. 6. Measured noise figure and gain as a function of supply voltage at 60GHz.

Since Vf is affected by temperature, its dependence of LNA noise characteristics is interesting. For the ambient temperature range of 20 $\pm$ 50 °C,

the noise figure and gain variations were $\pm$ 0.5dB and $\mp$ 1.6dB, respectively.

V Conclusions

Design and performance of a single-biased 60GHz-band monolithic LNA were described. A diode-regulated bias circuit was introduced to reduce the drain current sensitivity to FET threshold voltage variations. For the best LNA, the average noise figure from 58 to 62GHz was 3.3dB with 18dB gain at 3V. At 5V, the noise figure was unchanged with a gain of 16dB at 60GHz. The developed MMIC LNA featuring a small chip size and an excellent noise performance as well as a single bias supply with a wide voltage range promises great applicability to low-cost millimeter-wave wireless systems.

Acknowledgments

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